Datasheet

G32F031x8

Arm® Cortex® -M0+ core-based 32-bit MCU

Version: V1.0

1 Product Characteristics

- **Core**
  - 32-bit Arm® Cortex®-M0+ core
  - Up to 64MHz working frequency
- **Memory and interface**
  - Flash: Up to 64KB
  - SRAM: 8KB
- **Clock**
  - HSICLK: Factory calibrated 64MHz RC oscillator
  - LSICLK: 32.768KHz RC oscillator
- **Power and power management**
  - V_{DD} range: 1.8~5.5V
  - Support power-on/power-off (POR/PDR）
  - Support programmable voltage detector (PVD)
- **Low power mode**
  - Support sleep, stop and standby modes
- **DMA**
  - 1 DMA with 2 channels
- **Debugging interface**
  - SWD
- **I/O**
  - Up to 29 I/O
  - All I/Os can be mapped to external interrupt vectors
  - Up to 29 I/O tolerating 5V inputs
- **Communication peripherals**
  - 1 USART,1 UART support LIN function
  - 1 SPI
  - 1 I2C
- **Analog peripherals**
  - 1 12-bit ADC, support up to 8+2 external channels and 5 internal channels, with conversion range from 0V~5V. Maximum sampling rate 1.78 MSPS
  - 4 programmable analog comparators (COMP)
  - 2 rail-to-rail operational amplifiers (OPAMP)
- **Timer**
  - 1 16-bit advanced timer that can provide 8-channel PWM output, support for deadband generation and brake inputs
  - 1 32-bit general-purpose timer with 4 independent channels for input capture, output comparison, PWM and pulse counting
  - 2 16-bit basic timer
  - 1 16-bit low-power timer
  - 2 watchdog timers: an independent watchdog IWDT and a window watchdog WWDT
  - 1 24-bit self-reducing SysTick Timer
- **Algorithm unit**
  - CRC
  - DIV
- **96-bit unique device ID**
- **Chip package**
  - LQFP32
  - QFN32
  - QFN24
  - QFN20
  - SSOP28
  - SSOP24

Contents

2 Product Information

See the following table for product functions and peripheral configuration.

Table 1 Functions and Peripherals

Product		**G32F031**					
Model		K8Tx(1)	K8Ux	E8Ux	F8Ux	G8S6	E8S6
Package		LQFP32	QFN32	QFN24	QFN20	SSOP28	SSOP24
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@64MHz					
Working voltage		1.8~5.5V					
Flash (KB)		64					
SRAM (KB)		8					
DMA		1					
GPIOs		29		23	19	26	22
Algorithm units	CRC	1					
	DIV	1					
Timers	16-bit advanced (ATMR)	1					
	32-bit general (GTMR)	1					
	16-bit basic (BTMR)	2					
	24-bit SysTick (SYSTICK)	1					
	Watchdog	2（IWDT+WWDT）					
	LPTMR	1					
Communication interfaces	U(S)ART	1+1					
	I2C	1					
	SPI	1					
12-bit ADC	Unit	1					
	External channel	8+2		6+2		8+2	6+2
	Internal channel	5					
Comparator		4					
Operational amplifier (OPAMP)		2					
Temperature sensor		1					
Operating temperature		Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ Junction temperature: -40℃ to 105℃/-40℃ to 125℃					

Notes：

（1）When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.
When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

3 Pin Information

3.1 Pin distribution

Figure 1 LQFP32 Pin Distribution Diagram

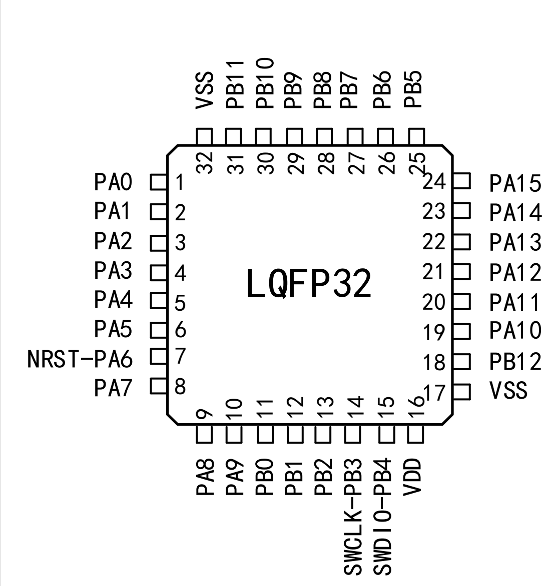


Figure 2 QFN32 Pin Distribution Diagram

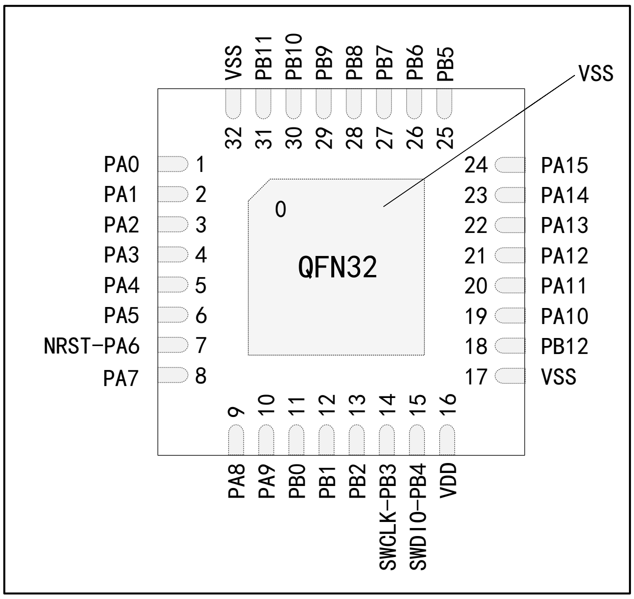


Figure 3 QFN24 Pin Distribution Diagram

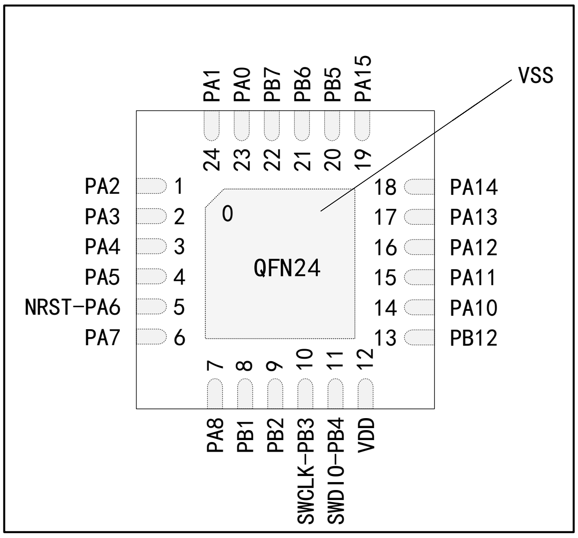


Figure 4 QFN20 Pin Distribution Diagram

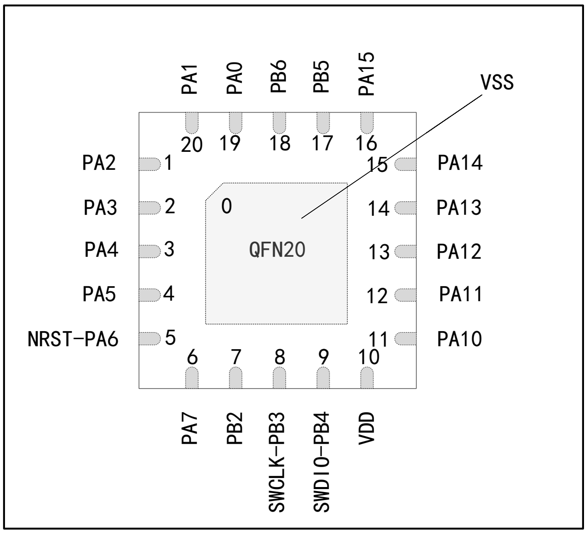


Figure 5 SSOP28 Pin Distribution Diagram

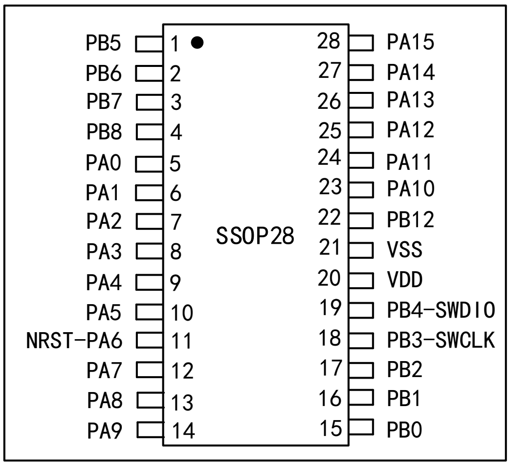
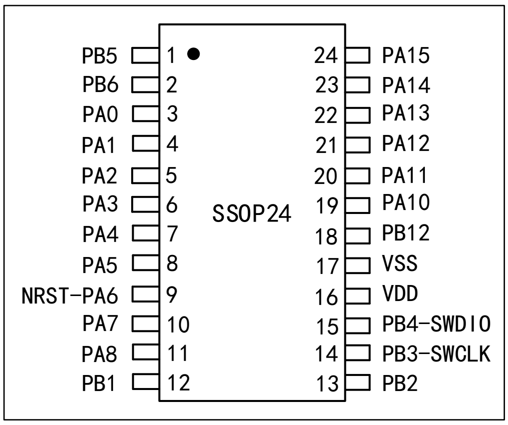


Figure 6 SSOP24 Pin Distribution Diagram



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power pin
		I	Only input pin
		O	Only output pin
		I/O	I/O pin
I/O structure		5T	5V tolerant FT I/O
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	One-way reset pin with built-in pull-up resistor
Notes		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Select this function through AFIO remapping registers	
	Additional function	Select this function directly through peripheral registers	

Table 3 Descriptions by Pin Number

LQFP32 /QFN32	QFN24	QFN20	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
1	23	19	5	3	PA0	USART_TX SPI_CS I2C_SCL	OPAMP0_OUT COMP3_INN	I/O(1)

LQFP32 /QFN32	QFN24	QFN20	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
2	24	20	6	4	PA1	USART_RX SPI_SCK I2C_SDA	OPAMP0_INN COMP1_INN	I/O
3	1	1	7	5	PA2	USART_CTS SPI_MOSI	OPAMP0_INP COMP2_INN	I/O
4	2	2	8	6	PA3	USART_RTS SPI_MISO	OPAMP1_INP	I/O
5	3	3	9	7	PA4	USART_CK	OPAMP1_INN	I/O
6	4	4	10	8	PA5	ATMR_BKIN COMP0_OUT	OPAMP1_OUT	I/O
7	5	5	11	9	NRST (PA6)	NRST	-	I/O
8	6	6	12	10	PA7	UART_TX I2C_SCL ATMR_BKIN GTMR_CH0_ETR BTMR1_CH0 WAKEUP0	ADC_IN0 COMP0_INP	I/O
9	7	-	13	11	PA8	UART_RX I2C_SDA ATMR_ETR GTMR_CH1 BTMR1_CH0 CLKOUT	ADC_IN1 COMP0_INN0	I/O
10	-	-	14	-	PA9	I2C_SMBA ATMR_CH3 GTMR_CH2 COMP1_OUT	ADC_IN2 COMP0_INN1	I/O
11	-	-	15	-	PB0	ATMR_CH3N GTMR_CH3 BTMR0_CH0 COMP1_OUT	ADC_IN3	I/O
12	8	-	16	12	PB1	UART_TX I2C_SDA ATMR_BKIN GTMR_CH0_ETR COMP0_OUT	ADC_IN4 COMP1_INN VREF+	I/O
13	9	7	17	13	PB2	UART_RX I2C_SCL ATMR_ETR GTMR_CH1 WAKEUP1	COMP2_INN	I/O

LQFP32 /QFN32	QFN24	QFN20	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
14	10	8	18	14	SWCLK (PB3)	SWCLK UART_TX ATMR_CH3N GTMR_CH2 BTMR0_CH0	-	I/O
15	11	9	19	15	SWDIO (PB4)	SWDIO UART_RX ATMR_CH3 GTMR_CH3 BTMR1_CH0	-	I/O
16	12	10	20	16	VDD	Digital power	-	P
17	0	0	21	17	VSS	Chip ground	-	P
18	13	-	22	18	PB12	USART_RTS SPI_MOSI ATMR_CH3 GTMR_CH2 BTMR1_CH0 COMP2_OUT	ADC_IN5	I/O
19	14	11	23	19	PA10	USART_TX ATMR_CH2N(2)	-	I/O
20	15	12	24	20	PA11	USART_RX ATMR_CH2(2)	-	I/O
21	16	13	25	21	PA12	USART_CTS SPI_CS ATMR_CH1N(2)	-	I/O
22	17	14	26	22	PA13	USART_RTS SPI_SCK ATMR_CH1(2)	-	I/O
23	18	15	27	23	PA14	USART_CK SPI_MOSI ATMR_CH0N(2)	-	I/O
24	19	16	28	24	PA15	SPI_MISO ATMR_CH0(2) BTMR1_CH0	-	I/O
25	20	17	1	1	PB5	UART_TX SPI_CS GTMR_CH2 COMP2_OUT	ADC_IN6 COMP3_INN	I/O
26	21	18	2	2	PB6	UART_RX SPI_SCK I2C_SMBA	ADC_IN7 COMP123_INP	I/O

LQFP32 /QFN32	QFN24	QFN20	SSOP28	SSOP24	Pin Name (After reset)	Digital Multiplexing Function	Analog Multiplexing Function	Type
						GTMR_CH3		
27	22	-	3	-	PB7	UART_TX SPI_MISO I2C_SCL GTMR_CH1 BTMR0_CH0 COMP1_OUT	-	I/O
28	-	-	4	-	PB8	UART_RX SPI_MOSI I2C_SDA GTMR_CH0_ETR BTMR1_CH0	-	I/O
29	-	-	-	-	PB9	USART_TX SPI_CS ATMR_BKIN GTMR_CH3 COMP2_OUT	COMP0_INP	I/O
30	-	-	-	-	PB10	USART_RX SPI_SCK ATMR_ETR GTMR_CH0_ETR COMP0_OUT	-	I/O
31	-	-	-	-	PB11	USART_CTS SPI_MISO ATMR_CH3N GTMR_CH1 BTMR0_CH0 COMP1_OUT	-	I/O
32	0	0	-	-	VSS	Chip ground	-	P

3.3 GPIO multiplexing configuration

Table 4 Multiplexing configuration for port A

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Secondary function	Analog
PA0	USART_TX	SPI_CS	I2C_SCL	-	-	-	-	-	-	OPAMP0_OUT COMP3_INN
PA1	USART_RX	SPI_SCK	I2C_SDA	-	-	-	-	-	-	OPAMP0_INN COMP1_INN
PA2	USART_CTS	SPI_MOSI	-	-	-	-	-	-	-	OPAMP0_INP COMP2_INN
PA3	USART_RTS	SPI_MISO	-	-	-	-	-	-	-	OPAMP1_INP
PA4	USART_CK	-	-	-	-	-	-	-	-	OPAMP1_INN
PA5	-	-	-	ATMR_BKIN	-	-	-	COMP0_OUT	-	OPAMP1_OUT
PA6	NRST(Default)	-	-	-	-	-	-	-	-	-
PA7	UART_TX	-	I2C_SCL	ATMR_BKIN	GTMR_CH0_ETR	BTMR1_CH0	-	-	WAKEUP0	ADC_IN0 COMP0_INP
PA8	UART_RX	-	I2C_SDA	ATMR_ETR	GTMR_CH1	BTMR1_CH0	-	CLKOUT	-	ADC_IN1 COMP0_INN0
PA9	-	-	I2C_SMBA	ATMR_CH3	GTMR_CH2	-	-	COMP1_OUT		ADC_IN2 COMP0_INN1
PA10	USART_TX	-	-	ATMR_CH2N(2)	-	-	-	-	-	-
PA11	USART_RX	-	-	ATMR_CH2(2)	-	-	-	-	-	-
PA12	USART_CTS	SPI_CS	-	ATMR_CH1N(2)	-	-	-	-	-	-
PA13	USART_RTS	SPI_SCK	-	ATMR_CH1(2)	-	-	-	-	-	-

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Secondary function	Analog
PA14	USART_CK	SPI_MOSI	-	ATMR_CH0N(2)	-	-	-	-	-	-
PA15	-	SPI_MISO	-	ATMR_CH0(2)	-	BTMR1_CH0	-	-	-	-

Table 5 Multiplexing configuration for port B

	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Secondary function	Analog
PB0	-	-	-	ATMR_CH3N	GTMR_CH3	BTMR0_CH0	-	COMP1_OUT	-	ADC_IN3
PB1	UART_TX	-	I2C_SDA	ATMR_BKIN	GTMR_CH0_ETR	-	-	COMP0_OUT	-	ADC_IN4 COMP1_INN VREF+
PB2	UART_RX	-	I2C_SCL	ATMR_ETR	GTMR_CH1	-	-	-	WAKEUP1	COMP2_INN
PB3	SWCLK（默认）	UART_TX	-	ATMR_CH3N	GTMR_CH2	BTMR0_CH0	-	-	-	-
PB4	SWDIO (默认)	UART_RX	-	ATMR_CH3	GTMR_CH3	BTMR1_CH0	-	-	-	-
PB5	UART_TX	SPI_CS	-	-	GTMR_CH2	-	-	COMP2_OUT	-	ADC_IN6 COMP3_INN
PB6	UART_RX	SPI_SCK	I2C_SMBA	-	GTMR_CH3	-	-	COMP3_OUT	-	ADC_IN7 COMP123_INP
PB7	UART_TX	SPI_MISO	I2C_SCL	-	GTMR_CH1	BTMR0_CH0	-	COMP1_OUT	-	-
PB8	UART_RX	SPI_MOSI	I2C_SDA	-	GTMR_CH0_ETR	BTMR1_CH0	-	-	-	-
PB9	USART_TX	SPI_CS	-	ATMR_BKIN	GTMR_CH3	-	-	COMP2_OUT	-	COMP0_INP
PB10	USART_RX	SPI_SCK	-	ATMR_ETR	GTMR_CH0_ETR	-	-	COMP0_OUT	-	-
PB11	USART_CTS	SPI_MISO	-	ATMR_CH3N	GTMR_CH1	BTMR0_CH0	-	COMP1_OUT	-	-
PB12	USART_RTS	SPI_MOSI	-	ATMR_CH3	GTMR_CH2	BTMR1_CH0	-	COMP2_OUT	-	ADC_IN5

Table 6 Configuration of the GPIOA_AF3RMP register

bit3:0	PA10 PWM multiplex	000：ATMR_CH0 001：ATMR_CH1 010：ATMR_CH2 011：ATMR_CH0N 100：ATMR_CH1N 101：ATMR_CH2N(Default)
bit7:4	PA11 PWM multiplex	000：ATMR_CH0 001：ATMR_CH1 010：ATMR_CH2(Default) 011：ATMR_CH0N 100：ATMR_CH1N 101：ATMR_CH2N
bit11:8	PA12 PWM multiplex	000：ATMR_CH0 001：ATMR_CH1 010：ATMR_CH2 011：ATMR_CH0N 100：ATMR_CH1N(Default) 101：ATMR_CH2N
bit15:12	PA13 PWM multiplex	000：ATMR_CH0 001：ATMR_CH1(Default) 010：ATMR_CH2 011：ATMR_CH0N 100：ATMR_CH1N 101：ATMR_CH2N

bit19:16	PA14 PWM multiplex	000：ATMR_CH0 001：ATMR_CH1 010：ATMR_CH2 011：ATMR_CH0N(Default) 100：ATMR_CH1N 101：ATMR_CH2N
bit23:20	PA15 PWM multiplex	000：ATMR_CH0(Default) 001：ATMR_CH1 010：ATMR_CH2 011：ATMR_CH0N 100：ATMR_CH1N 101：ATMR_CH2N

Note:

(1) all IO support 5V.

(2) PA10 ~ PA15 multiplex by GPIOA_AF3RMP register other ATMR channel configuration.

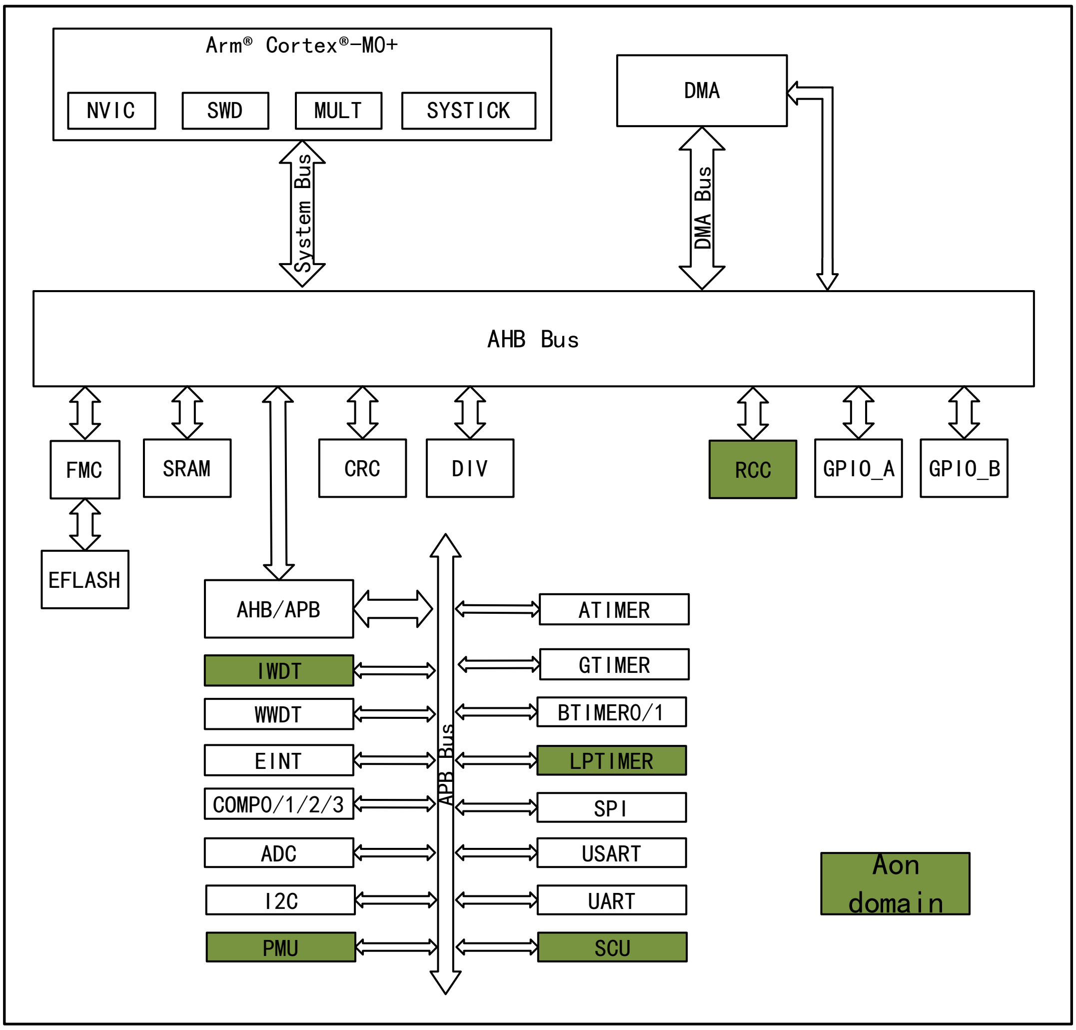
4 Functional Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of G32F031 series of products. For information about the Arm® Cortex®-M0+ core, refer to the *Arm® Cortex®-M0+ Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System Architecture

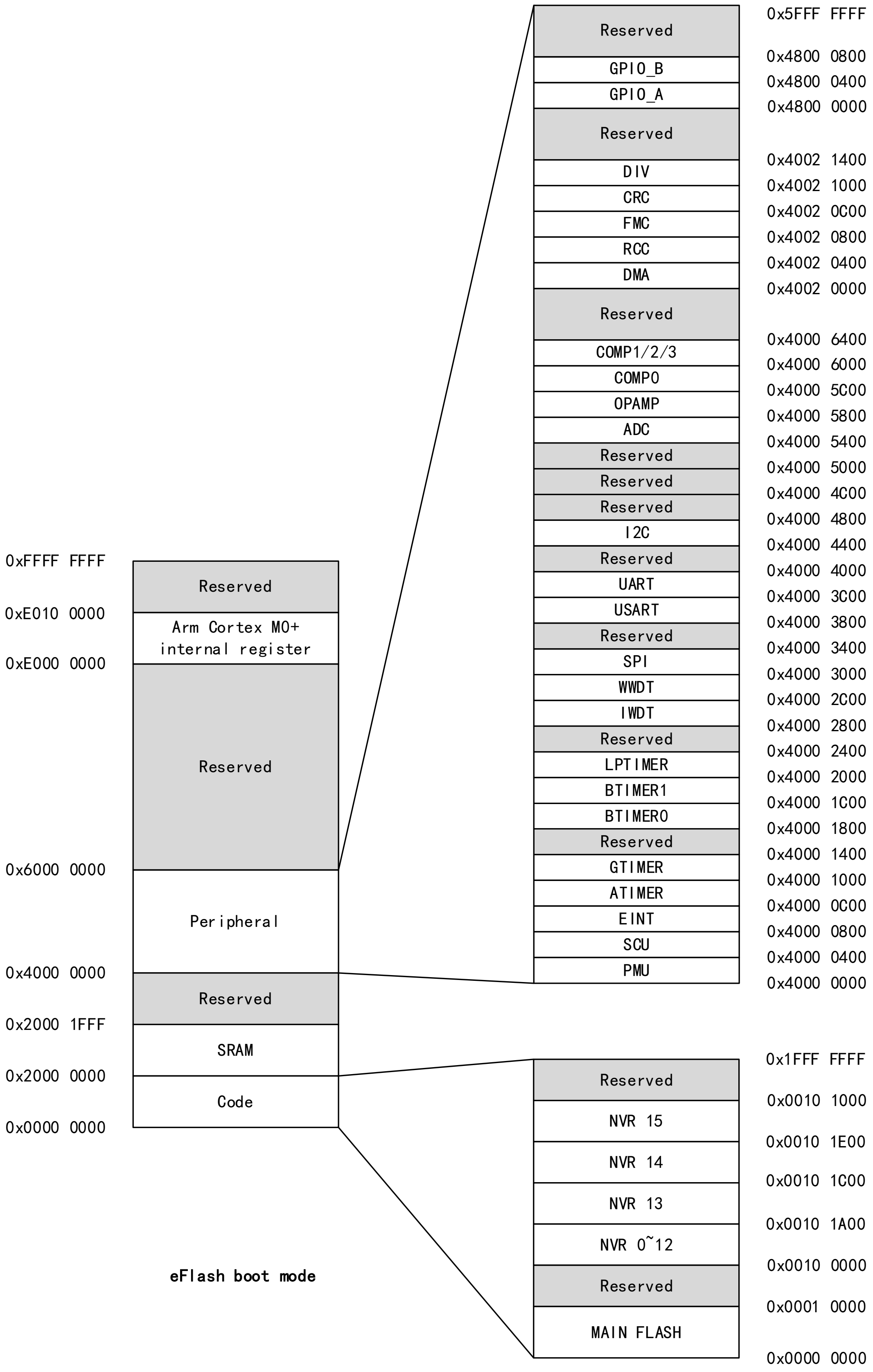
4.1.1 System Block Diagram

Figure 7 System Block Diagram



4.1.2 Address Mapping

Figure 8 Address Mapping



4.1.3 Start boot mode

The chip is activated by the Main memory (Main Flash). The main memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.

4.2 Core

The core of G32F031 is Arm® Cortex®-M0+, with its own MULT. based on a platform with low development cost, low power consumption, excellent computing performance and advanced system interrupt response. It is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

1 built-in NVIC and it is capable of handling up to 32 maskable interrupt channels and 4 priority levels. It can pass the interrupt vector entry address directly to the core to achieve low-latency interrupt response processing to prioritize the late arrival of higher priority interrupts.

4.3.2 External Interrupt/Event Controller (EINT)

External interrupt/event controller has 18 edge detectors, each detector contains edge detection circuitry, interrupt/event request generation circuitry; each detector can be configured as a rising-edge triggered, falling-edge, double-edge triggered, but also able to individually mask. Up to 29 GPIOs can be connected to 16 external interrupt lines.

4.4 On-chip memory

The on-chip memory includes the main storage area, SRAM, and user area.

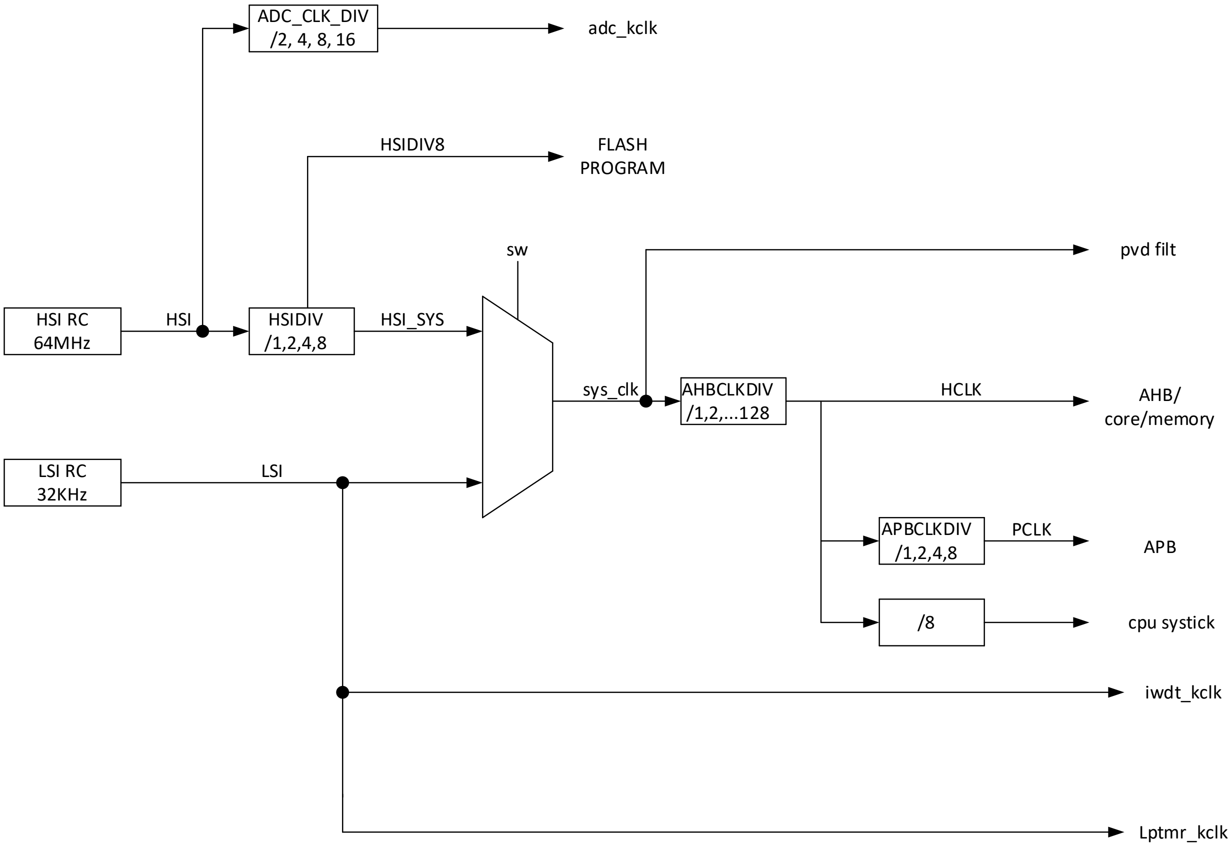
Table 7 On-chip Memory

Memory	Maximum Capacity	Function
Main memory area	64KB	Storage for user programme and data
SRAM	8 KB	CPU can access (read/write) with 0 cycles
User area	512 Bytes	Configuration of read/write protection of main memory area

4.5 Clock

4.5.1 Clock tree

Figure 9 Clock Tree



4.5.2 Clock sources

Clock source is divided into high-speed clock HSICLK and low-speed clock LSICLK according to the speed. In addition, some modules have additional clock source pins to obtain the required clock frequency through external circuits.

4.5.3 System clock

When the product is reset and started, HSICLK is started as the system clock by default, and if the interrupt is enabled, the software can receive the corresponding interrupt.

4.5.4 Bus clock

Built-in AHB, APB bus, the clock source of AHB is SYSCLK, and the clock source of APB is HCLK. Configure the dividing coefficient to obtain the required clock. The maximum frequency of AHB and APB is 64 MHz.

4.6 Power and power management

4.6.1 Power solution

Table 8 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	1.8~5.5V	Supplies power to I/O (see pin diagram for specific I/O), and internal regulator through V_{DD} pin.

Note: It is recommended to use 10uF and 100nF capacitors in parallel at the V_{DD} terminal.

4.6.2 Voltage regulator

Table 9 Regulator Operating Mode

Name	Description
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode

Note: The regulator is always in working state after reset.

4.6.3 Power supply voltage detector

Power-on reset (POR), power-down reset (PDR) are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit detects that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage detector (PVD) that monitors V_{DD} and compares it to the V_{PVD} threshold, and generates an interrupt when V_{DD} is outside of the V_{PVD} threshold range. The MCU can be set to a safe state through the interrupt service.

4.7 Low power mode

G32F031 supports three low-power modes, which are sleep mode ,stop mode and standby mode. There are differences in power consumption, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual requirements.

Table 10 Low Power Mode

Mode	Description
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode. The clock of the internal 5V power supply stops. HSICLK is disabled, and LSICLK is enabled. The voltage regulator can be configured to normal mode or low-power mode. The MCU can be woken up by any external interrupt line.
Standby mode	The power in this mode is the lowest;

Mode	Description
	The internal voltage regulator is disabled, all 1.5V power supply modules are powered down, LSICLK and HSICLK clocks are disabled, SRAM and register data disappears, and the standby circuit still works; The external reset signal on NRST, edge on WKUP pin or RTC event will wake up MCU to exit the standby mode.

4.8 DMA

A built-in DMA supports two DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, I2C, USART, UART, GTMR. Five levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

The maximum driving capability of GPIO is 6mA. It can be configured as general input mode, general output mode, multiplexing function mode, and analog input and output mode. General-purpose input can be configured as high-impedance. General-purpose output can be configured as push-pull and open-drain output. Multiplexing functions can be used for digital peripherals. Analog input and output can be used for analog peripherals as well as for low-power modes. Pull-up/down resistors can be configured to enable/disable the pull-up/pull-down resistors. A maximum of 20MHz can be configured, and the higher the speed, the larger the power consumption and the higher the noise will be. Supports schmitt inputs.

4.10 Communication peripherals

4.10.1 USART/UART

1 built-in general-purpose synchronous/asynchronous transceiver and 1 general-purpose asynchronous transceiver, with the communication rate at 8Mbit/s. All USART/UART can be configured with baud rate, parity bit, stop bit, data bit length, and can support DMA. The comparison of various USART/UART functions is shown in the table below:

Table 11 Comparison of supported functions between USART and UART

USART Mode	USART	UART
Half-duplex (single-line mode)	√	√
Automatic baud rate detection	√	√
Multiprocessor communication	√	-
Wake up from mute mode	√	-
Oversampling rate	8 times /16 times	16 times
Baud rate	8Mbit/s	4Mbit/s

USART Mode	USART	UART
Synchronization mode	√	-
LIN mode	√	√
Hardware flow control	√	-
RS485 driver enable	√	-
Multi-buffer communication (DMA)	√	√
Receiver timeout interrupt	√	√
Modbus communication	√	-

Note:√ means support.

4.10.2 I2C

I2C bus interfaces are built-in and they all can work in multiple-master or slave modes, support 7-bit or 10-bit addressing, supports standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (1Mbit/s); and can use DMA controllers. The I2C interface supports 7-bit or 10-bit addressing and dual-address addressing.

In addition, I2C also provides hardware support for SMBUS2.0 and PMBUS1.1: ARP function, master notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alert protocol management.

4.10.3 SPI

1 built-in SPI, supports full-duplex and half-duplex communication in both master and slave modes. DMA controller can be used, with a maximum communication rate of 16Mbps.

4.11 Analog peripherals

4.11.1 ADC

1 built-in ADC with 12-bit accuracy, with up to 8+2 external channels and 5 internal channels. The internal channels measure the temperature sensor voltage and internal reference voltage, OPAMP0/1 and 1/2VDD respectively. The A/D conversion modes of each channel are single, continuous or intermittent, and the ADC conversion results can be left-aligned or right-aligned stored in the data register. Segmented sampling is supported. DMA is supported.

4.11.1.1 Temperature sensor

1 built-in temperature sensor (TSensor), accuracy ±5℃. The voltage generated by the sensor varies linearly with the temperature, and can be converted to temperature by acquiring the converted voltage value from ADC.

Table 12 Tsensor Calibration Value

Calibration value name	Description	Address
V_{sensor_CAL}	Raw data collected at 25℃, V_{DDA}=5V(±10mV)	0x0010 1C14

4.11.1.2 Internal reference voltage

1 built-in internal reference voltage V_{BG}, and the V_{BG} voltage value can be obtained through the ADC. Meanwhile, the internal reference voltage is programmable and can be used as the positive input of COMP and the built-in bias voltage of OPAMP.

Table 13 Calibration Value of Internal Reference Voltage

Calibration value name	Description	Address
V_{BG_CAL}	Raw data collected at 25℃(±5℃), V_{DDA}=5V(±10mV)	0x0010 1C1C

4.11.2 Comparator（COMP）

4 built-in fast rail-to-rail comparators, support internal/external reference voltage, hysteresis, rate, programmable function, and configurable output polarity. Reference voltage can be selected from external I/O, internal reference voltage (V_{BG}), internal reference voltage 1/2. It can generate interrupts and simultaneously wake up the Sleep mode.

4.11.3 Operational amplifier（OPAMP）

It is equipped with 2 rail-to-rail OPAMPs with magnification ratios of 1,4,6,8,10,12 and 16 times. The output mode can be selected, with built-in biases of 1/2 VDDA, 1/4 VDDA, BG or 1/4 BG.

4.12 Timer

1 built-in 16-bit advanced timer ATIMER, 1 32-bit general-purpose timer GTIMER, 2 16-bit basic timer BTIMER, 1 low-power timer LPTIMER,1 stand-alone watchdog timer, 1 window watchdog timer, and 1 24-bit self-reducing system tick timer.

The watchdog timers can be used to check if a programme is running correctly.

The system tick timer is a peripheral of the core with an auto-reload function that generates a maskable system interrupt when the counter is 0. It can be used for a real-time operating system and time delay.

Table 14 Advanced/General/Basic/Low Power Timer Function Comparison

Item	Specific content/ Category	Advanced Timer	General Timer	Basic Timer	Low Power Consumption Timer
Name	-	ATIMER	GTIMER	BTIMER	LPTIMER
Time-based unit	Counter	16-bit	32-bit	16-bit	16-bit
	Prescaler	16-bit	16-bit	16-bit	16-bit
	Counting Mode	Up Down Center alignment	Up Down Center alignment	Up Down Center alignment	Up
Channel	Input Channel	0	4	1	0
	Capture Compare Channel	4	4	1	0

Item	**Specific content/ Category**	**Advanced Timer**	**General Timer**	**Basic Timer**	**Low Power Consumption Timer**
	Output channel	8	4	1	0
	Complementary output channel	4 groups	0	0	0
Function	Generate DMA request	No	Yes	No	No
	PWM mode	Yes	Yes	Yes	No
	Single pulse mode	Yes	Yes	Yes	No
	Forced output mode	Yes	Yes	Yes	No
	Deadband insertion	Yes	No	No	No

Table 15 IWDT and WWDT Comparison

Name	Counter resolution	Counter type	Prescaler factor	Function description
IWDT	12-bit	Down	Any integer between 1 and 256	The clock provided by an internal independent 32.768KHz RC oscillator. Because this RC oscillator is independent of the main clock, it can operate in stop modes. In case of problems, can reset the system. Can be used as a flexible timer to provide timeout management for applications.
WWDT	7-bit	Down	1/2/4/8	Can be set to run flexibly. In case of problems, can reset the system. Driven by the main clock with early warning interrupt function.

4.13 CRC

1 built-in CRC (Cyclic Redundancy Check) computing unit, which can generate CRC codes and can operate on 16-bit, and 32-bit data.

4.14 DIV

Include four 32-bit data registers that store divisor, dividend, quotient, and remainder respectively. It supports both signed and unsigned division.

5 Electrical Characteristics

5.1 Test Conditions of Electrical Characteristics

All voltage parameters (unless otherwise specified) refer to V_{SS}.

5.1.1 Maximum and Minimum Values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line. On the basis of comprehensive evaluation, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values after passing the sample test.

5.1.2 Typical values

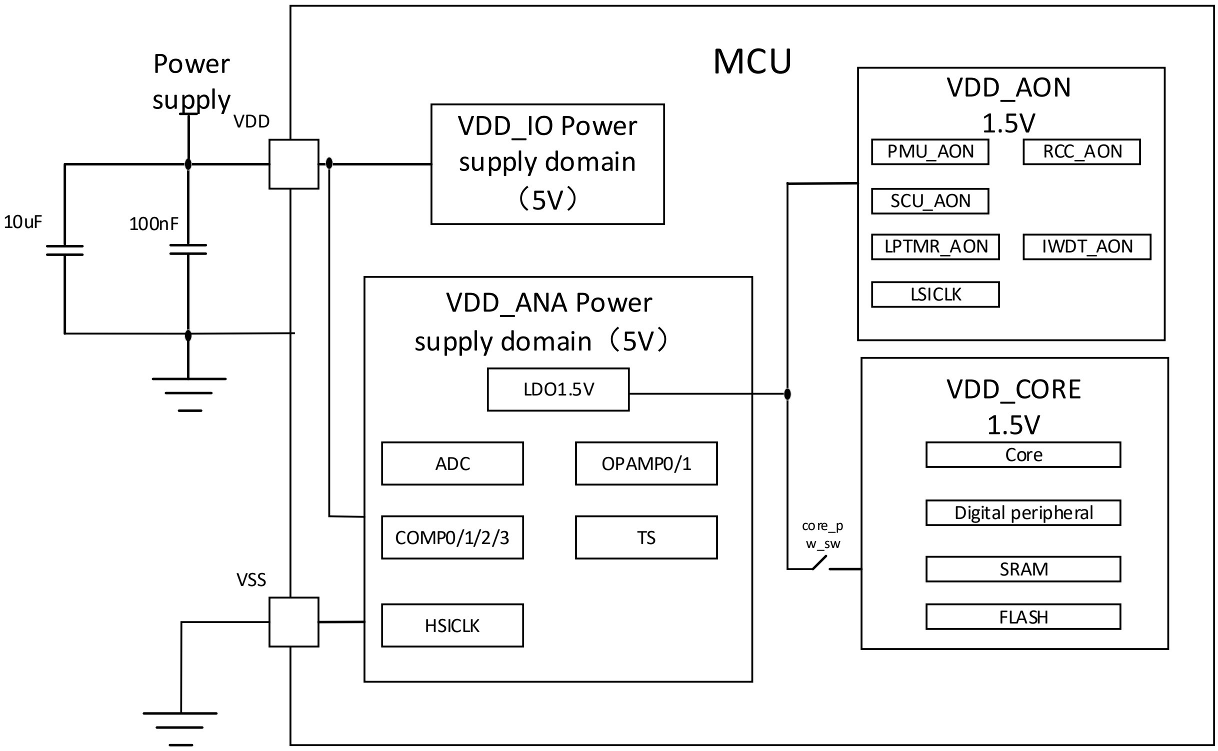
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=5V. these data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

5.1.4 Power Supply Scheme

Figure 10 Power Supply Scheme



5.1.5 Load Capacitance

Figure 11 Load Conditions when Measuring Pin Parameters

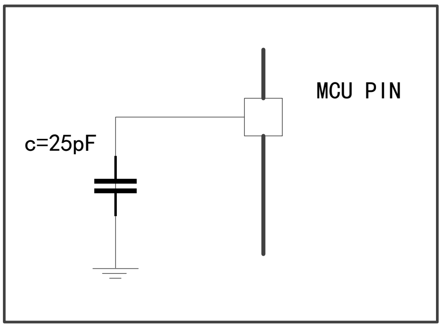


Figure 12 Pin Input Voltage Measurement Scheme

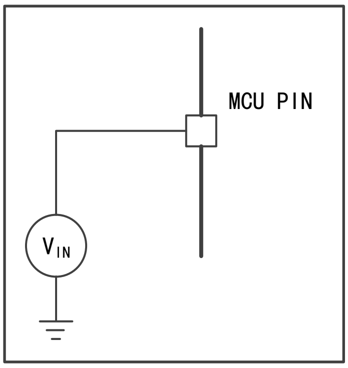
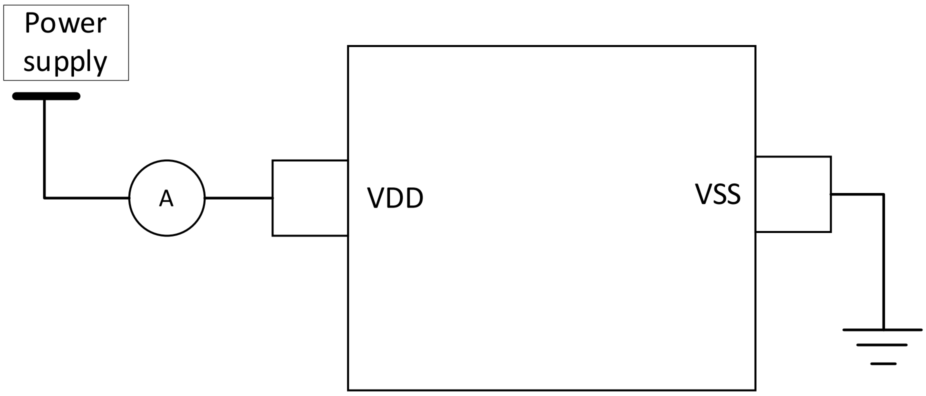


Figure 13 Power Consumption Measurement Scheme



5.2 Testing under General Working Conditions

Table 16 General Working Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	64	MHz
f_{PCLK}	Internal APB clock frequency	-	-	64	
V_{DD}	Power supply voltage input	-	1.8	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{DD}+0.3	V

5.3 Absolute Maximum Rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum Temperature Characteristics

Table 17 Temperature Characteristics

Symbol	Description	Numerical value	Unit
T_{STG}	Storage temperature range	–65~150	℃
T_J	Maximum junction temperature	125	℃

5.3.2 Maximum Rated Voltage Characteristics

All power supply and ground pins must always be connected to the power supply within the external limited range.

Table 18 Maximum Rated Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}	Power supply voltage input	2.7	5.5	V

5.3.3 Maximum Rated Current Characteristics

Table 19 Maximum Rated Current Characteristics

Symbol	Description	Max	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (1)	75	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (1)	75	
$I_{IO（PIN）}$	Output current sunk by any I/O and control pin	+6	
	Output current source by any I/O and control pin	-6	
$I_{INJ(PIN)}$(2)	Injected current on NRST pins	0/+6	
$\Sigma I_{INJ(PIN)}$	Total injected current (other pins)(3)	±24	

（1） All main power and ground pins must always be whitin the permitted range.

（2） If V_{IN} exceeds its maximum value, an external limit must be imposed on $I_{INJ(PIN)}$ not to exceed its maximum value. When $V_{IN}> V_{DDIOx}$, current flows into the pin. When $V_{IN}<V_{SS}$, current flows out of the pin.

（3） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4 ESD Characteristics

Table 20 ESD Characteristics

Symbol	Parameter	Condition	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (manikin)	T_A=+25℃, Standard: ANSI/ESDA/JEDEC JS-001-2017	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A=+25℃, Standard: ANSI/ESDA/JEDEC JS-002-2018	2000	

Note: It is tested by a third-party testing organization instead of in production.

5.3.5 Latch-up

Table 21 Latch-up

Symbol	Parameter	Condition	Max
LU	Class of static latch	T_A=105℃	Class II A

Note: It is tested by a third-party testing organization instead of in production.

5.4 On-Chip Memory

5.4.1 Flash Characteristics

Table 22 Flash Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{prog}	32 bit programming time	T_A=-40~105℃	-	60	-	μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ERASE}	Page(512B) erase time	T_A=-40~105℃	-	2.45	-	ms
t_{ME}	Whole erase time	T_A=25℃	-	30	-	ms
V_{prog}	Programming voltage	T_A=-40~105℃	2	-	5.5	V
t_{RET}	Data saving time	T_A = 125℃	10	-	-	years
N_{RW}	Erase cycle	T_A=-40~105℃	100K	-	-	cycles

Note: It is tested in comprehensive evaluation instead of in production.

5.5 Clock System

5.5.1 Characteristics of Internal Clock Source

High speed internal (HSICLK)RC oscillator

Table 23 HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSICLK}	Frequency	-		-	64	-	MHz
ACC_{HSICLK}	Accuracy of HSICLK oscillat	Factory calibration	V_{DD}=5V，T_A=25℃(1)	-0.5	-	0.5	%
			V_{DD}=2-5.5V，T_A=-40~105℃	-3	-	3	%
			V_{DD}=1.8-2V，T_A=-40~105℃	-5	-	5	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=5V T_A=-40~105℃		-	-	10	μs
$I_{DD(HSICLK)}$	Power consumption of HSICLK oscillator	-		-	350	499	μA

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

Low speed internal (LSICLK)RC oscillator

Table 24 LSICLK Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSICLK}	Frequency	V_{DD}=5V，T_A=25℃	31	32.768	34	KHz
$t_{SU(LSICLK)}$	Startup time of LSICLK oscillator	V_{DD}=1.8~5.5V，T_A=-40~105℃	-	75	-	μs
$Acc_{(LSICLK)}$	Accuracy of LSICLK oscillator		-30	-	30	%
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator		-	0.62	0.65	μA

Note: It is tested in comprehensive evaluation instead of in production.

5.6 Power Management

5.6.1 Power-on/power-down characteristics

Table 25 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	10	-	200000	μs/V
	V_{DD} fall time rate		20	-	200000	

5.6.2 Characteristic test of embedded reset and power control module

Table 26 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$ (1)	Power-on/power-down reset threshold	Falling edge	1.542	1.625	1.686	V
		Rising edge	1.594	1.676	1.738	V
$V_{PDRhyst}$	PDR hysteresis	-	-	50	-	mV
LVD	-	-	1.67	-	1.80	V

Note: It is tested in comprehensive evaluation instead of in production.

（1）PDR detector monitors V_{DD} and V_{DDA} (if enabled in option byte), POR detector monitors V_{DD} only.

Table 27 Programmable Voltage Detector Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[2:0]=000 (rising edge)	1.96	2.00	2.05	V
		PLS[2:0]=000 (falling edge)	1.86	1.90	1.95	V
		PLS[2:0]=001 (rising edge)	2.35	2.40	2.46	V
		PLS[2:0]=001 (falling edge)	2.25	2.30	2.36	V
		PLS[2:0]=010 (rising edge)	2.74	2.80	2.87	V
		PLS[2:0]=010 (falling edge)	2.64	2.70	2.77	V
		PLS[2:0]=011 (rising edge)	3.13	3.20	3.28	V
		PLS[2:0]=011 (falling edge)	3.03	3.10	3.18	V
		PLS[2:0]=100 (rising edge)	3.52	3.60	3.69	V
		PLS[2:0]=100 (falling edge)	3.42	3.50	3.58	V
		PLS[2:0]=101 (rising edge)	3.91	4.01	4.11	V
		PLS[2:0]=101 (falling edge)	3.81	3.90	4.00	V
		PLS[2:0]=110 (rising edge)	4.30	4.40	4.51	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		PLS[2:0]=110 (falling edge)	4.20	4.30	4.41	V
		PLS[2:0]=111 (rising edge)	4.68	4.80	4.91	V
		PLS[2:0]=111 (falling edge)	4.59	4.70	4.81	V
$V_{PVDhyst}$	PVD hysteresis	-	-	100	-	mV

Note: It is tested in comprehensive evaluation instead of in production.

5.6.3 BG

Table 28 BG characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBG	BG voltage	V_{DD}=5.5V，T_A=-40~105℃	1.19	-	1.27	V
Ibias	BG current		-	2	-	μA
TS_BG	Sampling time of the ADC when reading the internal reference voltage	-	10	-	-	μs
VBG_s	Built-in reference voltage extends to the temperature range	V_{DD}=5V	-	5	10	mV
Tcoeff	Tmperature coefficient	-	-	50	100	ppm/℃

5.7 Power Consumption

5.7.1 Power consumption test environment

(1) Test under the conditions of Coremark, KeilV5 compiling environment and L3 compiling optimization level.

(2) All I/O pins are configured as analog inputs, which are connected to VDD or V_{SS} (non-load) at a static level.

(3) Unless otherwise specified, all peripherals are turned off.

(4) The relationship between the setting of flash waiting period and f_{HCLK}:

0~16MHz: 0 waiting periods,
16~32MHz: 1 waiting periods,
32~64MHz: 2 waiting periods.

(5) Instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).

(6) When the peripheral is turned on: f_{PCLK}=f_{HCLK}.

5.7.2 Running mode

Table 29 The program is executed in Flash, and the power consumption in running mode

Parameter	**Condition**	**f_{HCLK}**	**Typ(1)**	**Max(1)**
			T_A=25℃，V_{DD}=3.3V	**T_A=105℃，V_{DD}=5.5V**
			I_{DD}(mA)	**I_{DD}(mA)**
Power consumption in running mode	HSECLK bypass，enabling all peripherals	64MHz	5.29	5.54
		32MHz	3.33	3.54
		16MHz	2.61	2.83
		8MHz	1.91	2.07
	HSECLK bypass，turn off all peripherals	64MHz	3.53	3.75
		32MHz	2.41	2.57
		16MHz	2.15	2.28
		8MHz	1.59	1.74

Note: (1)It is tested in comprehensive evaluation instead of in production.

Table 30 Power Consumption in Sleep mode when the program is executed in Flash

Parameter	**Condition**	**f_{HCLK}**	**Typ(1)**	**Max(1)**
			T_A=25℃，V_{DD}=3.3V	**T_A=105℃，V_{DD}=5.5V**
			I_{DD}(mA)	**I_{DD}(mA)**
Power consumption in sleep mode	HSECLK bypass, enabling all peripherals	64MHz	2.63	2.64
		32MHz	2.36	2.53
		16MHz	1.79	1.93
		8MHz	1.48	1.63
	HSECLK bypass, turn off all peripherals	64MHz	1.78	1.92
		32MHz	1.46	1.58
		16MHz	1.28	1.41
		8MHz	1.20	1.32

Notes: (1) It is tested in comprehensive evaluation instead of in production.

Table 31 Power Consumption in stop mode

Parameter	Condition		Typ(1),(T_A=25℃)			Max(1), (T_A=105℃)	Unit
			V_{DD}=1.8V	V_{DD}=3.3V	V_{DD}=5.5V	V_{DD}=5.5V	
Power Consumption in stop mode	V_{DD}	The kernel and most peripheral devices stop running, while IO, SRAM, and registers remain.	3.5	3.7	4.0	20.0	μA

Parameter	Condition		Typ(1),(T_A=25℃)			Max(1), (T_A=105℃)	Unit
			V_{DD}=1.8V	V_{DD}=3.3V	V_{DD}=5.5V	V_{DD}=5.5V	
Power Consumption in standby mode		1.5V power is turned off	1.7	1.8	2.0	5.0	

Notes: (1) It is tested in comprehensive evaluation instead of in production.

5.8 Wake-up Time in Low Power Mode

The measurement of wake-up time with low power consumption is from the start of wake-up event to the time when the user program reads the first instruction.

Table 32 Low Power Wake-up Time

Symbol	**Parameter**	**Condition**	**Min(1)**	**Typ(1) (T_A=25℃)**	**Max(1)**	**Unit**
$t_{WUSLEEP}$	Wake up from sleep mode	V_{DD}=5V	-	1	-	μs
t_{WUSTOP}	Wake up from stop mode		-	-	20	
$t_{WUSTANDBY}$	Wake up from standby mode		-	-	1000	

Note: (1) It is tested in comprehensive evaluation instead of in production.

5.9 I/O Port Characteristics

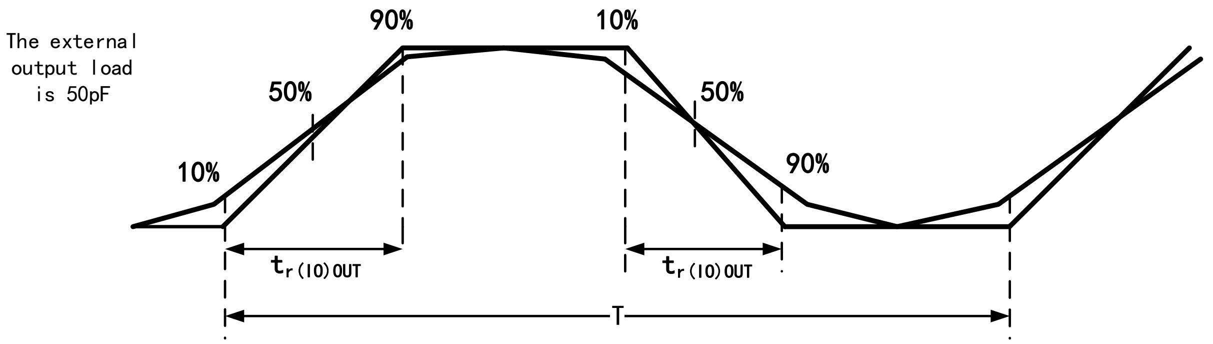
Table 33 DC Characteristics (T_A=-40℃-105℃)

Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input low level voltage	V_{DD}=5V	-	-	0.3V_{DD}	V
V_{IH}	Input high level voltage	V_{DD}=5V	0.7V_{DD}	-	-	V
V_{hys}	Schmitt trigger hysteresis	V_{DD}=5V	-	0.07V_{DD}	-	mV
I_{lkg}	Input leakage current	$V_{SS}≤V_{IN}≤V_{DDIOx}$	-	-	1	μA
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DDIOx}$	30	40	50	kΩ

Table 34 AC Characteristics (T_A =25℃)

Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
$f_{max(IO)out}$	Maximum frequency	C_L=25pF，V_{DD}=2.7~5.5V	-	-	20	MHz
$t_{f(IO)out}$	Output falling time from high to low level		-	-	15	ns
$t_{r(IO)out}$	Output rising time from low to high level		-	-	15	

Figure 14 Definition of Input and Output AC characteristics



If (tr+tf) is less than or equal to (2/3) T and the duty cycle is (45~55%)
When the load is 50pF, it reaches the maximum frequency

Table 35 Output Drive Current Characteristics (T_A =25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	I/O pin outputs low voltage	$\lvert I_{OLH}\rvert$=3mA, V_{DD}≥4.5V	-	-	0.4	V
V_{OH}	I/O pin outputs high voltage	$\lvert I_{OLH}\rvert$=2mA, V_{DD}≥2.7V	V_{DD}-0.4	-	-	
V_{OL}	I/O pin outputs low voltage	$\lvert I_{OLH}\rvert$=6mA, V_{DD}≥4.5V	-	-	0.4	
V_{OH}	I/O pin outputs high voltage	$\lvert I_{OLH}\rvert$=4mA, V_{DD}≥2.7V	V_{DD}-0.4	-	-	

Note: It is tested in comprehensive evaluation instead of in production.

5.10 NRST pin characteristics

The input drive of NRST pin adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}

Table 36 NRST Pin Characteristics (T_A =-40~105℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low voltage	V_{DD}=5V	-	-	0.3V_{DD}	V
$V_{IH(NRST)}$	NRST input high voltage	V_{DD}=5V	0.7V_{DD}	-	-	
$V_{hys(NRST)}$	Voltage hysteresis of NRST Schmitt trigger	V_{DD}=5V	-	0.07V_{DD}	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ

5.11 Communication Interface

5.11.1 I2C Interface Characteristics

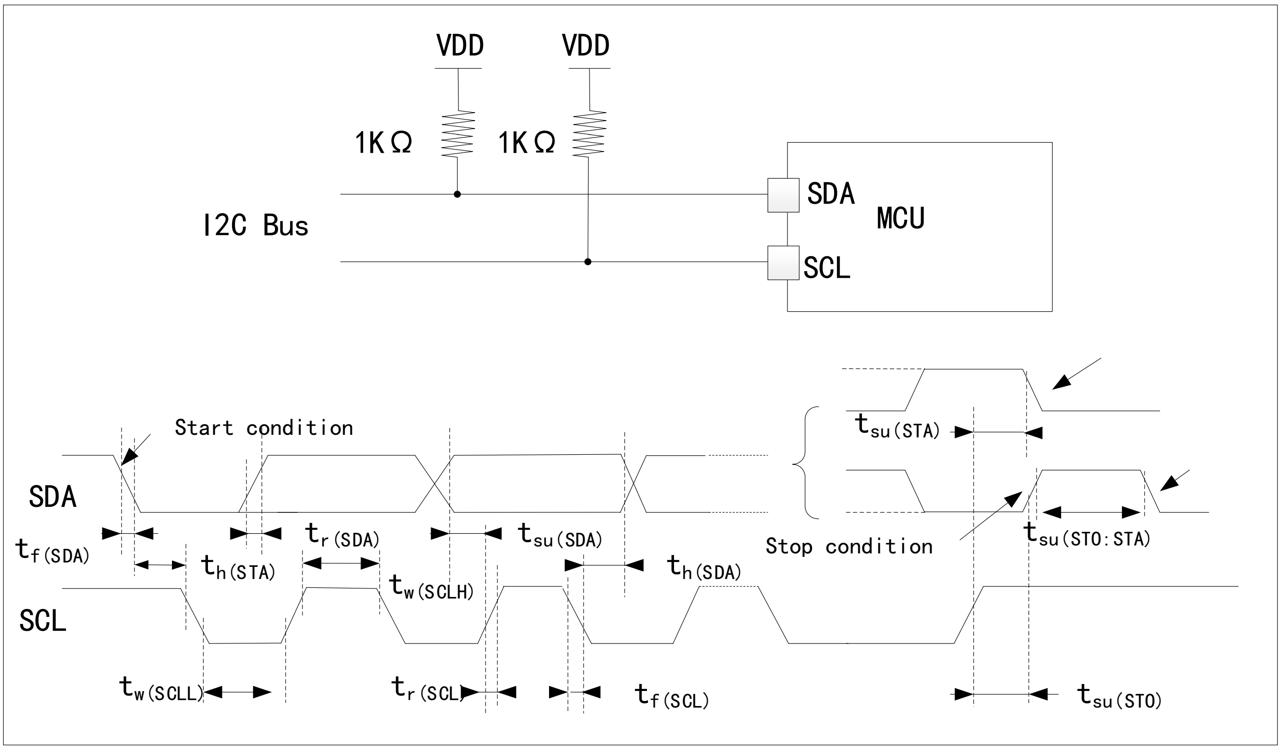
- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400kbit/s
- Ultrafast mode (Fm+): Up to 1Mbit/s

Table 37 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Ultrafast I2C		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	-	5.00	1.65	1.66	656.85	658.62	µs
$t_{w(SCLH)}$	SCL clock high time	-	4.96	789.35	790.49	290.91	292.17	
$t_{su(SDA)}$	SDA setup time	-	4.56	1.21	1.22	217.66	219.54	ns
$t_{h(SDA)}$	SDA data holding time	85.88	406.20	85.81	405.99	85.53	404.93	
$t_{r(SDA)}$	SDA rising time	30.24	31.63	30.96	31.53	30.32	31.45	
$t_{r(SCL)}$	SCL rising time	30.64	32.28	31.10	31.45	31.14	31.45	
$t_{f(SDA}$	SDA falling time	2.66	4.59	2.58	4.81	4.66	4.79	
$t_{f(SCL)}$	SCL falling time	5.18	5.40	5.28	5.40	5.34	5.50	
$t_{h(STA)}$	Start condition holding time	5.05	5.06	884.35	886.09	385.07	385.84	µs
$t_{su(STA)}$	Repeated start condition setup time	-	4.98	805.40	806.12	306.93	308.20	
$t_{su(STO)}$	Setup time of stop condition	-	9.99	2.46	2.47	969.51	970.96	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	711.81	713.14	398.95	399.40	570.44	572.58	µs
t_{AF}	Analog filter width	-	-	50	-	-	260	ns

Note: It is tested in comprehensive evaluation instead of in production.

Figure 15 Bus AC Waveform and Measurement Circuit



Note: the measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

5.11.2 SPI Interface Characteristics

Table 38 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode	-	-	20	
$t_{r(SCK)}$	SPI clock rising time	Load capacitance: C=15pF	2	-	7	ns
$t_{f(SCK)}$	SPI clock falling time		2	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK} + 10$	-	-	ns
$t_{w(SCKH)}$	SCK high time	Master mode, f_{PCLK} = 32 MHz, preassigned frequency coefficient = 4	21	-	32	ns
$t_{w(SCKL)}$	SCK low time		25	-	33	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	2	-	-	ns
		Slave mode	2	-	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	2	-	-	ns
		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK}=20MHz	-	-	15	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	-	-	18	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	12	-	25	ns
$t_{v(MO)}$		Master mode (after enable edge)	16	-	34	ns
$t_{h(SO)}$	Data output holding time	Slave mode (after enable edge)	11	-	16	ns
$t_{h(MO)}$		Master mode (after enable edge)	14	-	28	

Note: It is tested in comprehensive evaluation instead of in production.

Figure 16 SPI Timing Diagram—Slave Mode and CPHA=0

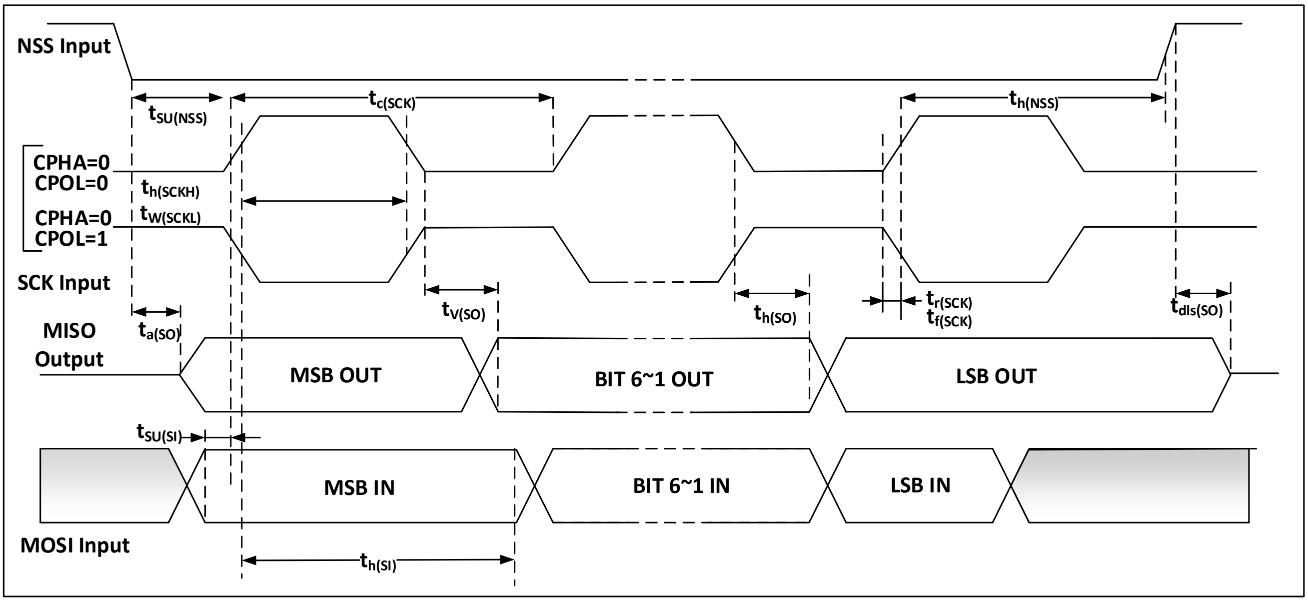
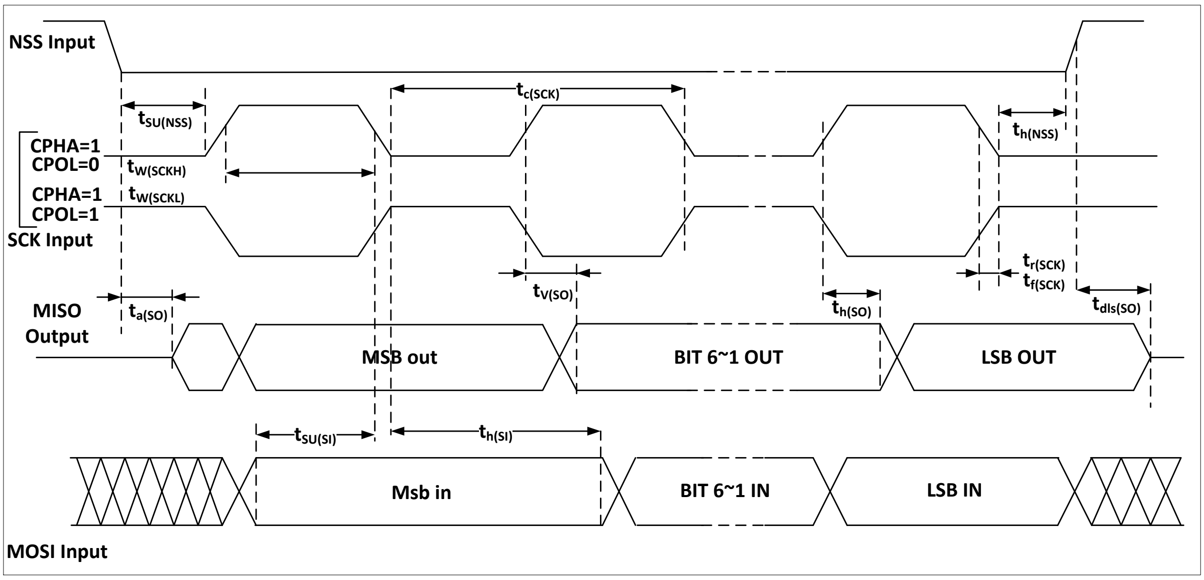
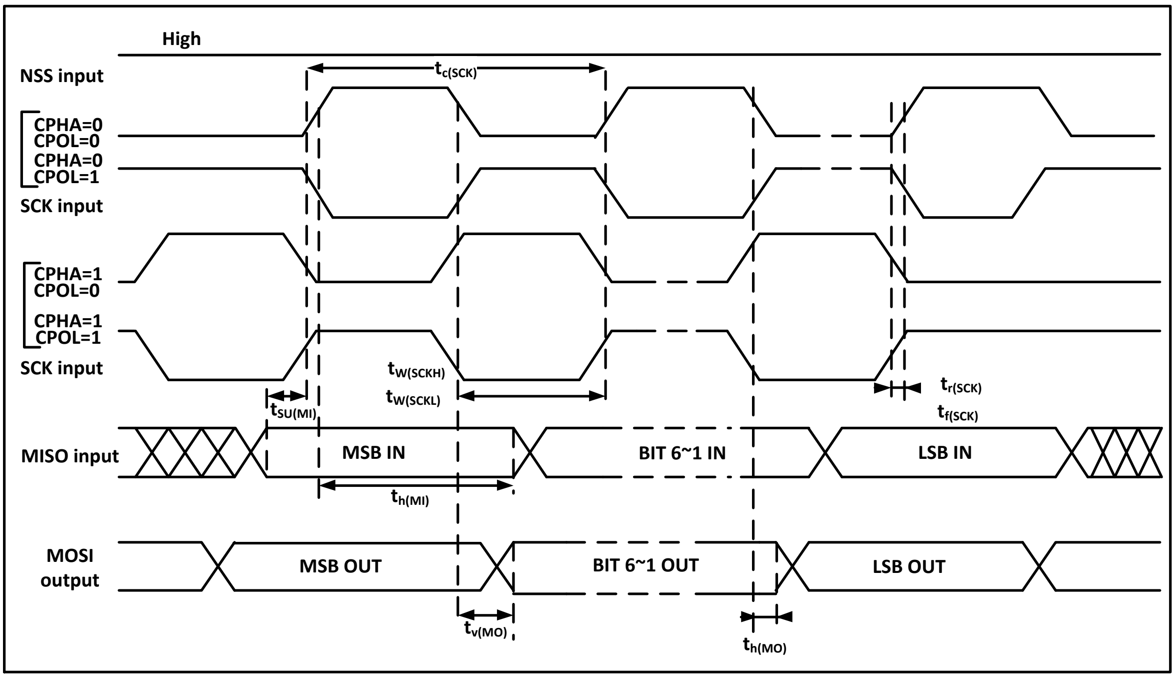


Figure 17 SPI Timing Diagram —Slave Mode and CPHA=1



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 18 SPI Timing Diagram—Master mode



Note: the measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.12 ADC

5.12.1 12-bit ADC Characteristics

Table 39 12-bit ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	standard voltage	2.7	-	5.5	V
		low voltage	2	-	2.7	V
		extra low voltage	1.75	-	2	V
F_{REQ}	Clock frequency	standard voltage	-	-	32	MHz
		low voltage	-	-	16	MHz
		extra low voltage	-	-	16	MHz
REF	Reference source	standard voltage	2.4	-	5.5	V
		low voltage	2	-	2.4	V
		extra low voltage	-	1.1	-	V
V_{AIN}	Input range	standard voltage	20	-	REF-20	mV
		low voltage	20	-	REF-20	mV
		extra low voltage	20	-	1080	mV
ENOB	Effective accuracy	standard voltage	-	10	-	BIT
		low voltage	-	9	-	BIT

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		extra low voltage	-	8	-	BIT
I_{DD}	Power dissipation	standard voltage	-	0.95	1.15	mA
		standard voltage low power	-	0.68	0.84	mA
		low voltage	-	0.58	0.73	mA
		extra low voltage	-	0.74	0.98	mA
PD	Electric leakage	standard voltage	-	30	9200	nA
R_{ADC}	Input resistance	NA	-	-	1000	Ω
C_{ADC}	Sampling capacitor	NA	-	1	-	pF
Fs	Sampling rate	NA	0.119	1.778	2	MHz
Ts	Sampling time	NA	31.25	93.75	7969	ns
T_{CONV}	Conversion time	NA	16	18	270	T
T_{SU}	Start-up time	NA	-	-	2	μs

Note: It is tested in comprehensive evaluation instead of in production.

Table 40 Accuracy of 12-bit ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
E_T	Composite error	standard voltage	0	±2.1	±3.9	LSB
		low voltage	0	±3.5	±5.3	
		extra low voltage	0	-	±80	
E_O	Offset error	standard voltage	0	±1.5	±2.5	
		low voltage	0	±2.5	±3.5	
		extra low voltage	0	±4.5	±6.5	
E_G	Gain error	standard voltage	0	±1.5	±3	
		low voltage	0	±2.5	±4	
		extra low voltage	0	-	±80	
E_D	Differential linear error	standard voltage	0	±1	±1.5	
		low voltage	0	±2	±2.5	
		extra low voltage	0	±3	±3.5	
E_L	Integral linearity error	standard voltage	0	±1.5	±2	
		low voltage	0	±2.5	±3	
		extra low voltage	0	±3.5	±4	

Note: It is tested in comprehensive evaluation instead of in production.

5.12.2 Temperature Sensor Characteristics

Table 41 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Slope	Average slope(V_{DD} = 5.5V，T_A = -40~105℃)	-	-3.802	-	mV/ºC
V25	Voltage at 25℃	-	1.36	-	V
Ts_temp	Sampling time of the ADC when reading the temperature	-	-	17.1	μs
TL	temperature departure	-	±5	-	℃

5.13 Comparator

Table 42 Comparator Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.7	5	5.5	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	-
V_{OUT}	Comparator output voltage range	-		0	-	V_{DDA}	V
t_D	propagation delay(The time it takes for the input flip to change to 50% of the output flip.)	-		-	150	200	ns
-	Operating current	T_A=-40~105℃/ V_{DD}=5.5V		-	350	450	μA
V_{OFFSET}	Offset voltage	-		-10	-	10	mV
V_{hys}	Hysteresis voltage	Hysteresis voltage control bit	00	-	0	-	mV
			01		±20		
			10		±40		
			11		±80		

Note: It is tested in comprehensive evaluation instead of in production.

5.14 Operational amplifier

Table 43 Operational amplifier Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	2.7	5	5.5	V
Closed-loop gain	Gain factor	Internal	1	-	16	factor
		External	1	-	32	
CMIR	Common-mode input range	-	-(V_{DDA}-300)/G	-	(V_{DDA}-300)/G	V
Voffset	Input offset voltage	-	-10	-	10	mV
IDDOPAMP	Current consumption	non-loaded	-	1	-	mA

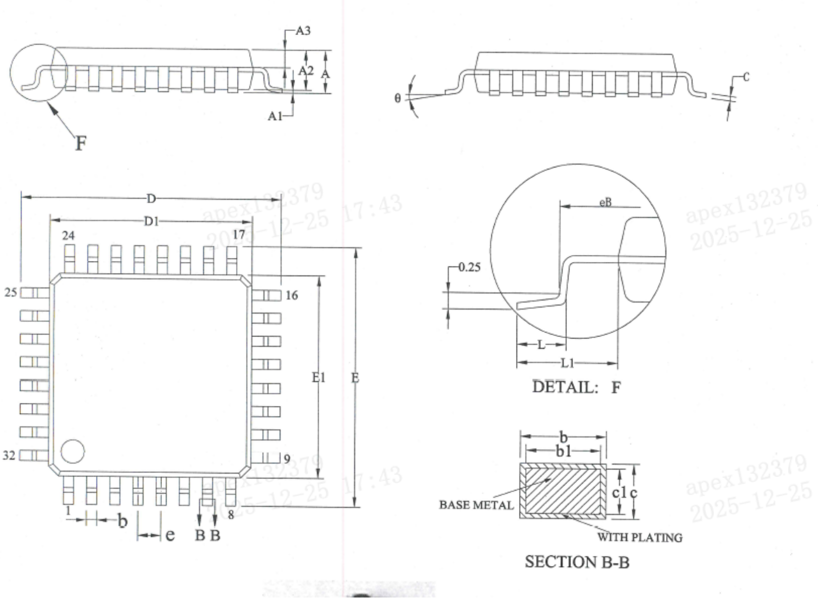
Symbol	Parameter	Condition	Min	Typ	Max	Unit
SR	Slew rate	CL=15pF, RL≥4KΩ,G=1	-	14	-	V/μs
Twakeup	Setup time from shutdown to wake-up	CL≤15pF, RL≥4KΩ, Internal gain G=1~16	-	1	2	μs
		CL≤15pF, RL≥4KΩ, External gain G=1~32	-	2	3	
VOHSAT	High saturation output voltage	CL≤15pF，RL=4KΩ	-	-	V_{DDA}-100	mV
VOLSAT	Low saturation output voltage		100	-	-	mV
-	Gain accuracy error		-2.5	-	2.5	%

Note: It is tested in comprehensive evaluation instead of in production.

6 Package Information

6.1 LQFP32 Package Information

Figure 19 LQFP32 Package Diagram

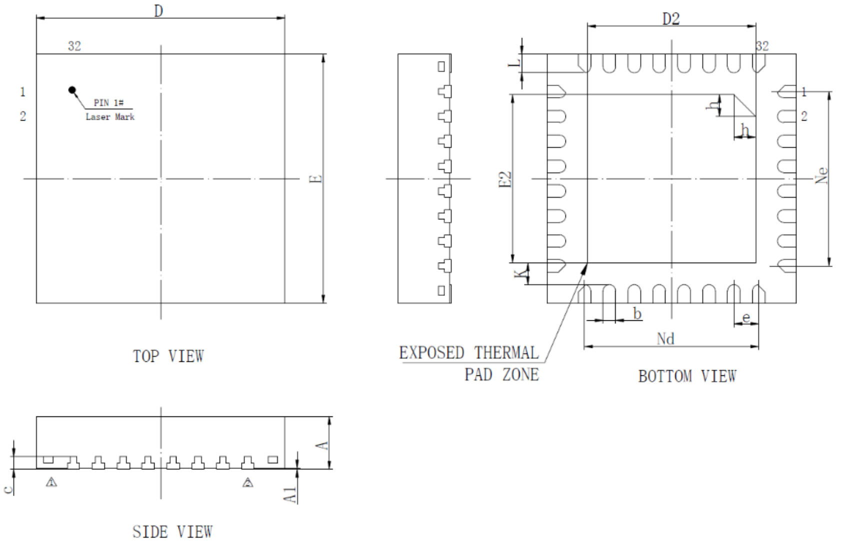


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Note: The figure is not drawn to scale.

6.2 QFN32 Package Information

Figure 20 QFN32 Package Diagram

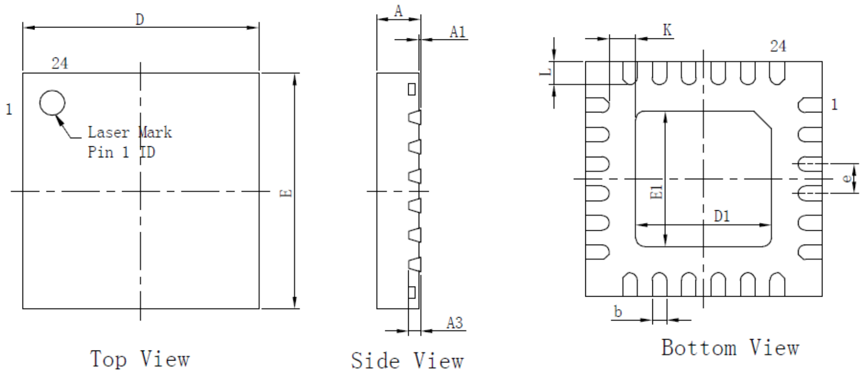


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0. 75	0. 80
A1	0	0. 02	0. 05
b	0. 15	0.20	0. 25
c	0. 203REF		
D	3. 90	4. 00	4. 10
D2	2. 60	2. 70	2. 80
e	0. 40BSC		
Nd	2. 80BSC		
E	3. 90	4. 00	4. 10
E2	2. 60	2. 70	2. 80
Ne	2. 80BSC		
L	0. 25	0. 30	0. 35
h	0. 30	0. 35	0. 40
K	0. 35REF		

Note:The figure is not drawn to scale.

6.3 QFN24 Package Information

Figure 21 QFN24 Package Diagram

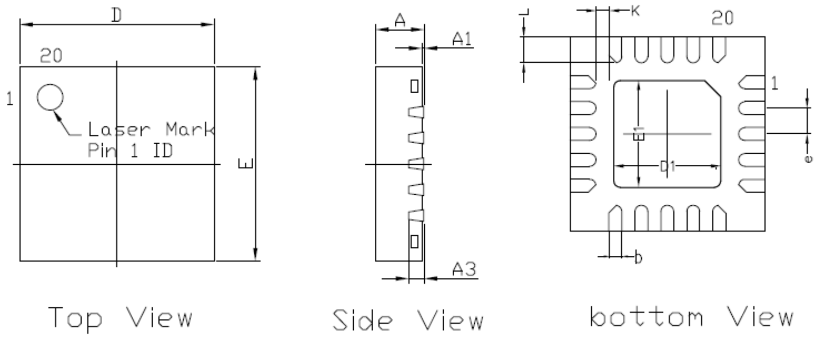


Standard \ Size	Min	Typ	Max
A	0. 70	0. 75	0. 80
A1	0. 00	—	0. 05
A3	0. 203REF		
b	0. 20	0. 25	0. 30
D	3. 90	4. 00	4. 10
E	3. 90	4. 00	4. 10
D1	2. 20	2. 30	2. 40
E1	2. 20	2. 30	2. 40
e	0. 50TYP		
K	0. 20	–	–
L	0. 30	0. 40	0. 50

Note:The figure is not drawn to scale.

6.4 QFN20 Package Information

Figure 22 QFN20 Package Diagram

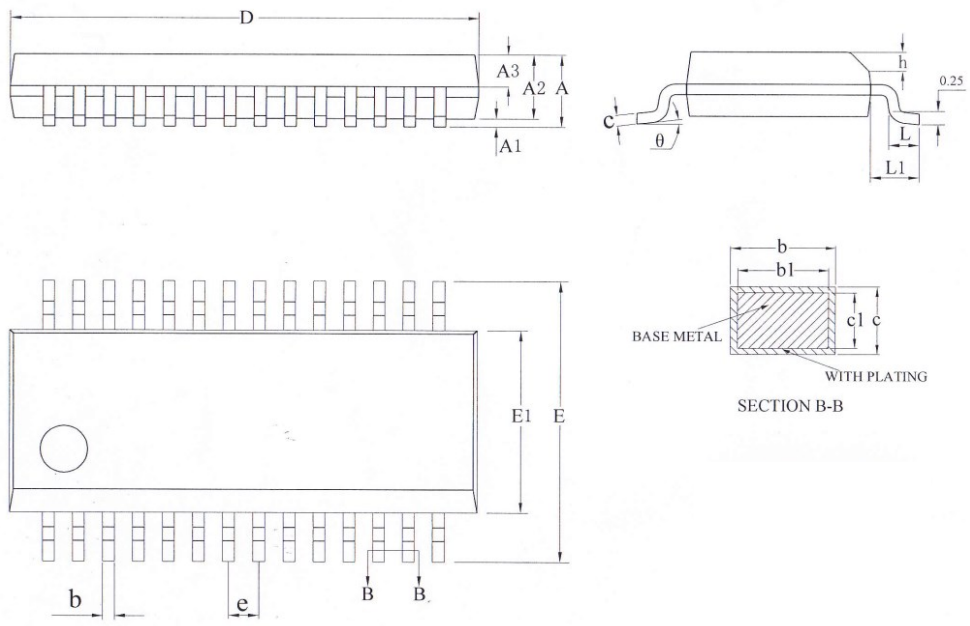


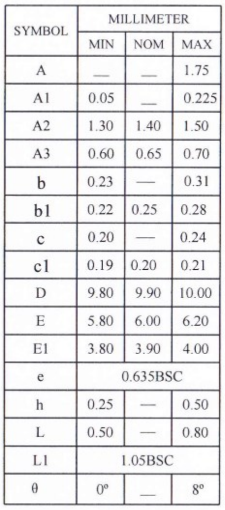
Standard \ Size	Min	Typ	Max
A	0. 70	0. 75	0. 80
A1	0. 00	—	0. 05
A3	0. 203REF		
b	0. 15	—	0. 25
D	2. 90	3. 00	3. 10
E	2. 90	3. 00	3. 10
D1	1. 55	1. 65	1. 75
E1	1. 55	1. 65	1. 75
e	0. 40TYP		
K	0. 20	-	-
L	0. 30	0. 40	0. 50

Note:The figure is not drawn to scale.

6.5 SSOP28 Package Information

Figure 23 SSOP28 Package Diagram



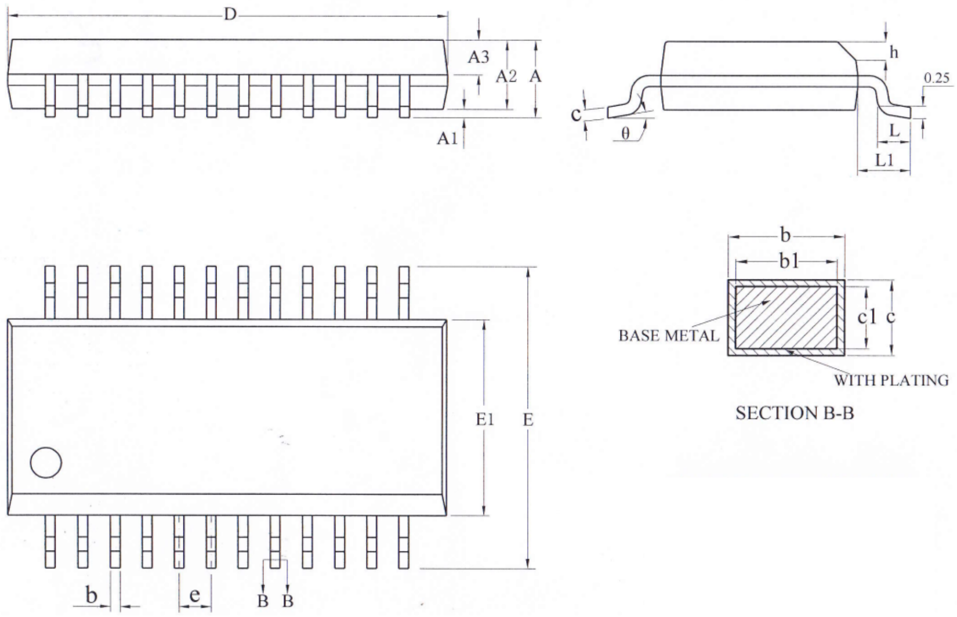


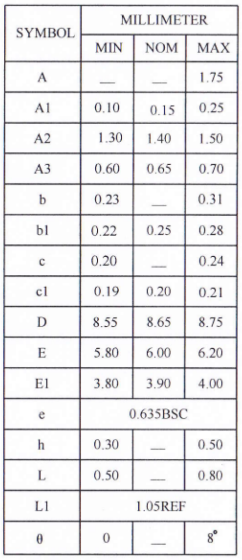
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Note:The figure is not drawn to scale.

6.6 SSOP24 Package Information

Figure 24 SSOP24 Package Diagram





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Note:The figure is not drawn to scale.

6.7 Package Designator

Figure 25 LQFP Package Designator

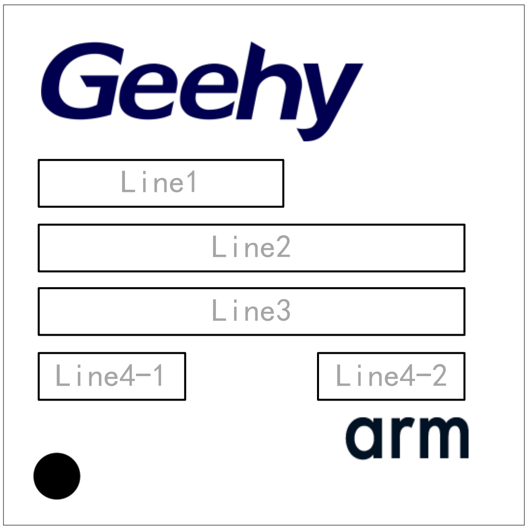


Table 44 LQFP silk-screen printing figure description

Symbols and Icons	description
Geehy	Geehy
Line1	Product Series
Line2	product model
Line3	batch number
Line4-1	Internal traceability code
Line4-2	Year and week number
arm	Arm® authorization identification
●	PIN1 location

Note: The number of digits in each column above is not fixed.

Figure 26 QFN Package Designator

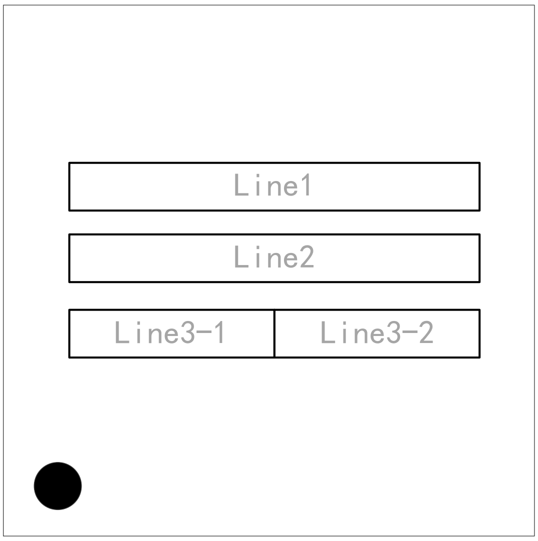


Table 45 QFN silk-screen printing figure description

Symbols and Icons	description
Line1	product model
Line2	batch number
Line3-1	Internal traceability code
Line3-2	Year and week number
●	PIN1 location

Note: The number of digits in each column above is not fixed.

Figure 27 SSOP Package Designator

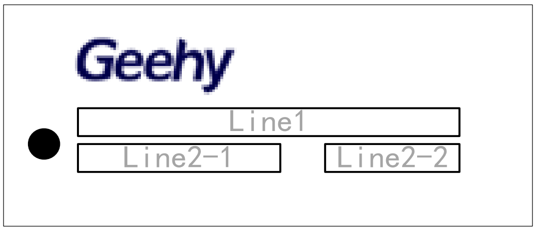


Table 46 SSOP silk-screen printing figure description

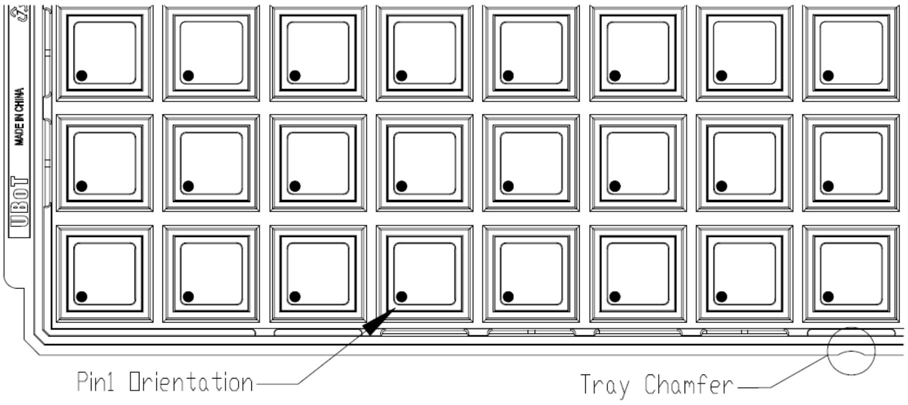
Symbols and Icons	description
Geehy	Geehy
Line1	product model
Line2-1	batch number
Line2-2	Year and week number
●	PIN1 location

Note: The number of digits in each column above is not fixed.

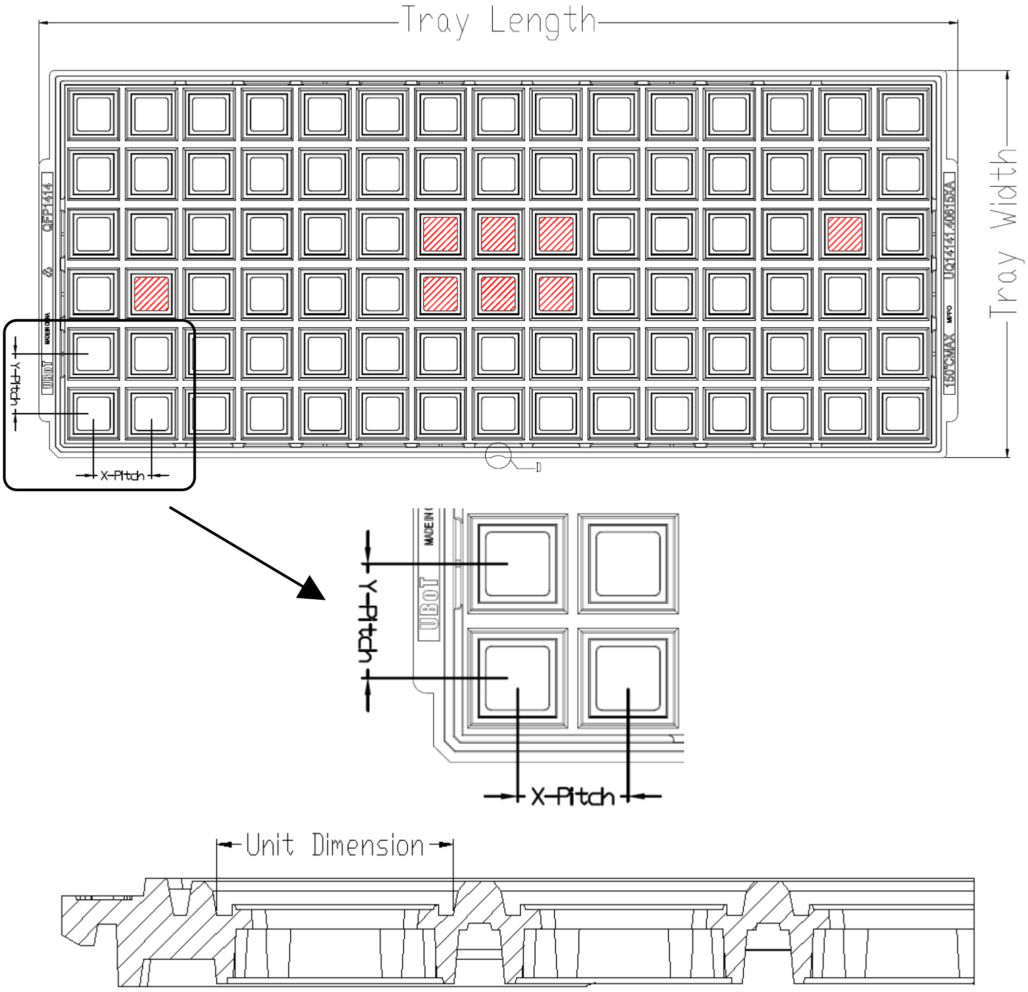
7 Packaging Information

7.1 Tray packaging

Figure 28 Tray Packaging Diagram



Tray Dimensions



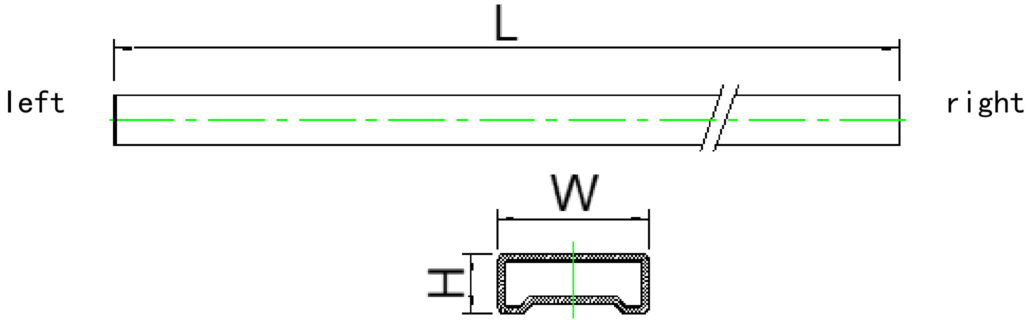
Note: All photos are for reference only, and the appearance is subject to the product.

Table 47 Parameter Specification Table of Pallet Packaging

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32F031K8T6	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32F031K8U6	QFN	32	4900	4.185	4.185	8.8	9.2	322.6	135.9
G32F031E8U6	QFN	24	4900	4.2	4.2	8.8	9.2	322.6	135.9
G32F031F8U6	QFN	20	6240	3.2	3.2	7.5	7.5	322.6	135.9
G32F031K8T7	LQFP	32	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32F031K8U7	QFN	32	4900	4.185	4.185	8.8	9.2	322.6	135.9
G32F031E8U7	QFN	24	4900	4.2	4.2	8.8	9.2	322.6	135.9
G32F031F8U7	QFN	20	6240	3.2	3.2	7.5	7.5	322.6	135.9

7.2 Tube packaging

Figure 29 Tube package drawing



Note: All photos are for reference only, and the appearance is subject to the product.

Table 48 Specification table of tube packaging parameters

Device	Package Type	Pins	SPQ	L(mm)	W(mm)	H(mm)
G32F031G8S6	SSOP	28	5000	520	7.8	3.4
G32F031E8S6	SSOP	24	5000	520	7.8	3.4

Note: SPQ= Smallest Package Quantity.

8 Ordering Information

Table 49 Product naming definition

product name			
G32F031K8T6			
Name Example	Definition	Name	Information
G32	Product Series	G32	Arm -based 32-bit MCU
F	Product type	F	Electrical machinery
031	Product subseries	031	General
G	Number of pins	F	20 pins
		E	24 pins
		G	28 pins
		K	32 pins
8	Flash memory capacity	8	64KB
T	Package	T	LQFP
		U	QFN
		S	SSOP
6	Temperature range	6	temperature range:-40℃~85℃
		7	temperature range:-40℃~105℃
T	pack	Blank	Tray packaging
		T	Tube packaging

Table 50 Ordering Information List

Order Code	**FLASH（KB）**	**SRAM（KB）**	**Package**	**SPQ**	**Temperature range**
G32F031K8T6	64	8	LQFP32	2500	-40℃~85℃
G32F031K8U6	64	8	QFN32	4900	-40℃~85℃
G32F031E8U6	64	8	QFN24	4900	-40℃~85℃
G32F031F8U6	64	8	QFN20	6240	-40℃~85℃
G32F031G8S6-T	64	8	SSOP28	5000	-40℃~85℃
G32F031E8S6-T	64	8	SSOP24	5000	-40℃~85℃
G32F031K8T7	64	8	LQFP32	2500	-40℃~105℃
G32F031K8U7	64	8	QFN32	4900	-40℃~105℃
G32F031E8U7	64	8	QFN24	4900	-40℃~105℃
G32F031F8U7	64	8	QFN20	6240	-40℃~105℃

9 Commonly Used Function Module Denomination

Table 51 Commonly Used Function Module Denomination

Full name	**Abbreviation**
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCC
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC Controller	CRC
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time Clock	RTC
External memory controller	EMMC
Controller Area Network	CAN
I2C Interface	I2C
Serial Peripheral Interface	SPI
Universal asynchronous receiver transmitter	UART
Universal synchronous and asynchronous receiver transmitter	USART
Flash interface control unit	FMC
Safe digital input/output	SDIO
Digital camera interface	DCI

10 Revision

Table 52 Document Revision History

Date	Version	Change History
September, 2025	1.0	• initial version

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